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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/911,581	07/25/2001	Takahiro Ohnakado	401308	6065

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LEYDIG VOIT & MAYER, LTD
700 THIRTEENTH ST. NW
SUITE 300
WASHINGTON, DC 20005-3960

EXAMINER	
RICHARDS, N DREW	

ART UNIT	PAPER NUMBER
2815	

DATE MAILED: 06/18/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/911,581	OHNAKADO, TAKAHIRO	
	Examiner	Art Unit	
	N. Drew Richards	2815	

-- The MAILING DATE of this communication appears on the cover sheet with th correspond nce address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *29 April 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-8 and 13-16* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *1-4* is/are allowed.

6)☒ Claim(s) *5,6,13 and 16* is/are rejected.

7)☒ Claim(s) *7,8,14 and 15* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *25 July 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 5, 6, 13 and 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ma et al. (U.S. Patent No. 5939753) in view of Wang (U.S. Patent No. 6351363 B1).

With regard to claims 5 and 6, Ma et al. disclose in figures 8 and 10, a substrate 11, a Si MOS transistor 115 and an ESD protection circuit 160 in high frequency devices a a capacitor having lower and upper polysilicon electrodes and the transistor having a polysilicon gate. Ma et al. do not disclose the ESD circuit having a first lateral polysilicon diode on the substrate, the first lateral polysilicon diode having a forward direction and a reverse direction, wherein the first lateral polysilicon diode connects, in the forward direction, a high-frequency I/O signal line to an externally supplied voltage VDD.

Wang teaches an ESD circuit. Wang teaches in figure 3, an ESD circuit comprising a first lateral polysilicon diode 11 on a substrate, the diode having a forward direction and a reverse direction, wherein the diode connects, in the forward direction, a

I/O signal line to an externally supplied voltage VDD. In combination, the diode of Wang would connect to a high-frequency I/O signal line of Ma et al.

Ma et al. teach the gate electrode being polysilicon and the first and second electrodes of the capacitor being polysilicon. Wang teach the diode being polysilicon. Ma et al. combined with Wang, the diode and lower electrode of the capacitor share a single first polysilicon layer and the upper electrode of the capacitor and the gate are from a second polysilicon layer. Whether formed simultaneously or in different steps, the limitation of the first lateral polysilicon diode and lower electrode of the capacitor being from a single first polysilicon layer and the polysilicon gate being from a second polysilicon layer as claimed only structurally requires the device to have the capacitor electrodes, gate, and diode formed of polysilicon. The first polysilicon layer of Ma et al. (lower capacitor electrode) and the second polysilicon layer of Ma et al. (gate electrode) have a different dopant impurity concentration. Though the dopant impurity concentrations are not explicitly disclosed, Ma et al. teach the lower capacitor electrode being doped when it is formed (col. 4 lines 18-20) and then after the gate electrode is formed the lower capacitor electrode is doped in each doping step that dopes the gate electrode. Thus, the lower capacitor electrode will have a higher dopant impurity concentration than the gate electrode.

Ma et al. and Wang are combinable because they are from the same field of endeavor. At the time of the invention it would have been obvious to a person of ordinary skill in the art to form a lateral polysilicon diode connected between the I/O signal line and Vdd as the ESD protection circuit. The motivation for doing so is the use

of lateral polysilicon diode provides faster ESD protection response as it is isolated from the substrate and has reduced parasistic substrate capacitance. Therefore, it would have been obvious to combine Ma et al. with Wang to obtain the invention of claims 5 and 6.

With regard to claim 13 and 16, Ma et al. disclose in figures 8 and 10, a substrate 11, a Si MOS transistor 115 and an ESD protection circuit 160 in high frequency devices a a capacitor having lower and upper polysilicon electrodes and the transistor having a polysilicon gate. Ma et al. do not disclose the ESD circuit having a first lateral polysilicon diode on the substrate, the first lateral polysilicon diode having a forward direction and a reverse direction, wherein the first lateral polysilicon diode connects, in the forward direction, ground to a high-frequency I/O signal line.

Wang teaches an ESD circuit. Wang teaches in figure 3, an ESD circuit comprising a first lateral polysilicon diode 11 on a substrate, the diode having a forward direction and a reverse direction, wherein the diode connects, in the forward direction, ground (VSS in figure 3, disclosed as ground on column 4 line 6) to an I/O signal line. In combination, the diode of Wang would connect to a high-frequency I/O signal line of Ma et al.

Ma et al. teach the gate electrode being polysilicon and the first and second electrodes of the capacitor being polysilicon. Wang teach the diode being polysilicon. Ma et al. combined with Wang, the diode and lower electrode of the capacitor share a single first polysilicon layer and the upper electrode of the capacitor and the gate are

from a second polysilicon layer. Whether formed simultaneously or in different steps, the limitation of the first lateral polysilicon diode and lower electrode of the capacitor being from a first polysilicon layer and the polysilicon gate being from a second polysilicon layer as claimed only structurally requires the device to have the capacitor electrodes, gate, and diode formed of polysilicon. The first polysilicon layer of Ma et al. (lower capacitor electrode) and the second polysilicon layer of Ma et al. (gate electrode) have a different dopant impurity concentration. Though the dopant impurity concentrations are not explicitly disclosed, Ma et al. teach the lower capacitor electrode being doped when it is formed (col. 4 lines 18-20) and then after the gate electrode is formed the lower capacitor electrode is doped in each doping step that dopes the gate electrode. Thus, the lower capacitor electrode will have a higher dopant impurity concentration than the gate electrode.

Ma et al. and Wang are combinable because they are from the same field of endeavor. At the time of the invention it would have been obvious to a person of ordinary skill in the art to form a lateral polysilicon diode connected ground and the signal line as the ESD protection circuit. The motivation for doing so is the use of a lateral polysilicon diode provides faster ESD protection response as it is isolated from the substrate and has reduced parasistic substrate capacitance. Therefore, it would have been obvious to combine Ma et al. with Wang to obtain the invention of claims 13 and 16.

Allowable Subject Matter

3. Claims 1-4 allowed. Applicant perfected their foreign priority on 11/3/03 to overcome the rejection of claims 1-4.

4. Claims 7, 8, 14 and 15 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Response to Arguments

5. Applicant's arguments filed 4/29/04have been fully considered but they are not persuasive. It is noted that bridging pages 6 and 7 of the response, at least one line of applicant's arguments has been cut off. The examiner will attempt to respond to the argument as best understood from the portions present. Applicant argues that since the polysilicon layers of Ma (for example, gate electrodes 53, 54, 55, upper and lower electrode of capacitor 57 and resistor layer 58) have different elevations the first lateral polysilicon diode and lower capacitor electrode cannot share a single first polysilicon layer. This is not persuasive. The claims are drawn towards a device and thus any limitation is interpreted in light of the structure claimed. Claiming the lower capacitor electrode and the first lateral polysilicon diode sharing a single first polysilicon layer does not structurally distinguish over the prior art where both structures are formed of polysilicon. Further, the elevation of the polysilicon layers has no bearing on the invention as claimed. The fact that different polysilicon layers have different elevations

does not necessitate the different layers being formed separately. Even if it did, since the claims are drawn towards a device the claim is not limited to forming the layers together or separately. As far as the structure claimed, the rejection is considered proper as the combination of references teach every limitation.

Conclusion

6. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to N. Drew Richards whose telephone number is (571) 272-1736. The examiner can normally be reached on M-F 8:00-5:30; Every other Friday off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas can be reached on (571) 272-1664. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

NDR

Tom Thomas

TOM THOMAS
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800